COMPUTER-AIDED DESIGN OF HIGHLY LINEAR, HIGH-POWER VARACTOR-TUNED FREQUENCY MODULATORS

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ABSTRACT

A systematic approach to the design of linear high-power varactor-tuned frequency modulators is presented. It is shown that a few simple measurements on the free-running oscillator together with a suitable use of modern general-purpose optimization programs allow the designer to predict and control all aspects of the design problem, including linearity of the frequency-voltage characteristic, the R.F. voltage swing across the varactor junction, and the optimum choice of the varactor diode itself.

Introduction

The problem of designing varactor-tuned transistor oscillators (VTO's) for microwave integrated circuits, even broad-band, has been extensively treated in literature, both in the FET and the bipolar transistor case[1-2] and can be considered as a relatively settled matter. When the VTO must act as a frequency modulator, linearity is primarily of concern, and the design problem gets harder. Though a number of methods for varactor linearization are well known to R&D engineers, a straightforward approach yielding solutions easy to be realized by MIC technology has not been presented so far. Thus except for the choice of a rough starting point suggested by previous experience, the design specifications are usually met by empirical trimming and trial-and-error techniques.
The problem is further complicated when the oscillator to be modulated is medium- or high-power, since the varactor junction must then be protected against an excess of R.F. voltage. If this is the case, empirically finding a solution may proof a lengthy and critical job.

It is the purpose of this paper to illustrate a possible systematic approach to the design of linear high-power VTO's, allowing all aspects of the design problem to be simultaneously taken into account. This method requires a few simple measurements on the free-running oscillator and the application of modern computer-aided design techniques.

Description of the method

As a starting point, let us refer to a transistor oscillator circuit having the standard topology shown in fig. 1.

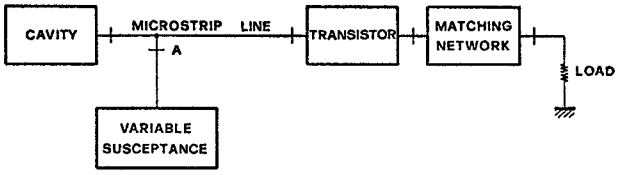

Fig. 1
Schematic of microstrip transistor oscillator

It is assumed that this network has been designed in such a way that a stable oscillation at a frequency f_0 takes place when port A is open-circuited, i.e., the variable susceptance connected to this port is zero. In this case the microstrip line merely acts as an impedance transformer allowing the correct feedback reactance to load the input port of the transistor. The resonant cavity may be realized by either microstrip or coaxial line depending on the noise requirements for the oscillator.

If a nonzero susceptance is now connected in parallel to the microstrip line in some section A, the frequency of oscillation will obviously be changed. We will denote by B(f) the susceptance value which is required in order to make the circuit oscillate at a specified frequency f.
To measure B(f) at a number of discrete frequency points, an open-circuited stub of known characteristic impedance may be connected to the main line in section A, and then etched away stepwise to change the frequency of oscillation. An analytical expression may then be obtained by a least-square fit procedure.
Moreover the magnitude of the R.F. voltage in section A at any given frequency, namely V(f), can be roughly evaluated by loosely coupling a power meter to the open end of the stub and relating the measured power to the input voltage by standard circuit algebra.
The knowledge of the functions of frequency B(f) and V(f) represents the starting point for the computer-aided design procedure to be described below.

To change the free-running oscillator into a VTO, a reactive network containing a varactor diode is connected to port A. In the most general case this network can be represented as in fig. 2, where $\mathcal{N}$ is a two-port including the linearizing network and the package parasitics of the varactor, while C_j is the junction capacitance of the reverse-biased varactor diode.

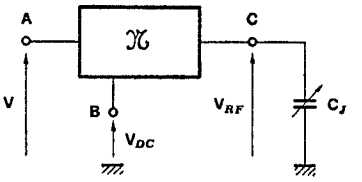

Fig. 2
Schematic of varactor tuning network

In fig. 2 port B represents the D.C. port through which the low-frequency modulating signal is fed to the varactor.
For simplicity the absence of losses will be assumed in the following, though the method is equally applicable to the case of lossy (i.e., finite-Q) varactor and linearizing network, at the expense of computer time.

Now the design goal may be stated as follows: it is required that the linearizing network be designed in such a way that

1) the frequency of oscillation of the transistor circuit be related to the applied D.C. voltage by

$$f = f_0 + S\,(V_{DC} - V_0)\,, \qquad (1)$$

where S is the modulation slope and V_0 is the reverse bias voltage of the varactor, throughout a prescribed frequency band $(f_1 \div f_2)$;

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2) in the above band the magnitude of the R.F. voltage across the varactor junction be low enough to avoid forward conduction and reverse breakdown, that is,

$$|V_{RF}(f)| < V_{DC}(f) - \Delta V$$
$$|V_{RF}(f)| + V_{DC}(f) < V_B - \Delta V \quad , \tag{2}$$

where V_B is the breakdown voltage and ΔV represents a suitably selected safety margin.

In order to apply any computer-aided design procedure, a suitable objective function must be defined. To do this, let us consider any frequency f within the range $(f_1 \div f_2)$.
If the VTO were working in exact agreement with the design specifications, the D.C. voltage across the varactor, required in order to make the circuit oscillate at frequency f, would be, from (1):

$$V_T = (f - f_0)/S + V_0 \quad . \tag{3}$$

On the other hand, the D.C. voltage that is *actually* required for any given topology of the linearizing network, can be readily computed. In fact, let

$$Y_{ik} = jB_{ik} \qquad (i,k = 1,2)$$

be the short-circuit admittance parameters of the two-port network in fig. 2 at frequency f. By definition the input admittance at port A must equal jB(f), so that the required junction capacitance of the varactor diode is given by

$$C_R = \{-B_{22} + \frac{B_{12}\,B_{21}}{B_{11} - B(f)}\}/2\pi f \quad . \tag{4}$$

Now let the varactor capacitance be related to the applied D.C. voltage by

$$C_j = F_c(V_{DC}) \quad . \tag{5}$$

The analytic form of (5) is usually given by the manufacturers for abrupt junctions, or may be obtained by a least-square fit from graphical data in the hyperabrupt case. We will assume that the correction due to the presence of R.F. drive[1] is included in (5).
Using (4) and the inverse of (5) the actual required voltage is immediately found:

$$V_A = F_c^{-1}(C_R) \quad . \tag{6}$$

Ideally one should have $V_A = V_T$, so that a first contribution to the objective function for network optimization can be chosen as

$$F_1(f) = |(V_A - V_T)/V_T| \quad . \tag{7}$$

(7) represents the contribution to the objective function arising from the first design specification at frequency f.

As specification 2) is concerned, note that the magnitude of the R.F. voltage across the junction can be readily expressed from fig. 2 as

$$|V_{RF}| = |\{B(f) - B_{11}\}/B_{12}| \cdot V(f) \quad , \tag{8}$$

so that a *normalized excess voltage* v_E can be defined in the form

$$v_E = \max \{(|V_{RF}| + \Delta V - V_A)/V_A \,,\; (|V_{RF}| + V_{DC} + \Delta V - V_B)/V_A\} \quad , \tag{9}$$

where ΔV and V_B are defined by (2).
Thus the contribution to the objective function at frequency f arising from the second design specification can be taken as

$$F_2(f) = \begin{cases} v_E \text{ if } v_E > 0 \\ 0 \text{ if } v_E \leq 0 \quad . \end{cases} \tag{10}$$

At this stage the objective function for a minimax optimization[3] can be formulated as follows:

$$F_{ob} = \max_{f_1 \leq f \leq f_2} \{F_1(f) + w\,F_2(f)\} \quad , \tag{11}$$

where w is a suitable weight whose choice is essentially related to the output power level of the oscillator. Alternatively a least-p^{th} formulation can be adopted as described in ref. 4.

Once a suitable topology has been selected for the linearizing network, the electrical parameters of the latter obviously represent the independent design variables.
For maximum design flexibility it is also convenient to treat the varactor reverse bias voltage V_0 and the modulation slope S as independent variables of the optimization process, with suitable lower and upper bounds. Furthermore note that, in many practical cases, families of varactor chips, having the same capacitance-voltage characteristic except for a constant multiplying factor, are available from the manufacturers (e.g., the ALPHA DKW 6533 A÷F family). These chips can fit into the same package, so that the mounting parasitics are the same no matter which particular one is being used. For such a family the capacitance-voltage relationship (5) may be given the form

$$C_j = K\,F_0(V_{DC}) \quad , \tag{12}$$

where F_0 is fixed and different K values correspond to different chips. Thus if K is used as an additional independent design parameter in the early steps of the optimization process, *even the best choice of the varactor diode can be demanded to the computer.*

As a final remark note that, for practical applications to FM transmission, one is often more interested in controlling the behavior of the modulation slope df/dV_{DC} as a function of frequency, rather than the straightness of the frequency-voltage characteristic itself. In fact it is the slope that essentially affects the intermodulation noise.
Now, while the direct optimization of the slope is usually not possible by standard CAD programs, the designer's control on it can nevertheless be enhanced by using a suitably distorted function instead of the straight line (3) as the optimization goal.
For instance, a common requirement is that the deviation of the modulation slope from the ideal constant value, S, be of the form

$$\frac{df}{dV_{DC}} - S = -4S\delta^2\{(f - f_0)/(f_2 - f_1)\}^2 \quad , \tag{13}$$

where δ^2 represents the maximum allowed fractional change of the slope at the band edges, and f_0 is the centre-band frequency.

A direct integration of (13) yields the theoretical frequency-voltage characteristic:

$$V_T = \frac{f_2 - f_1}{4S\delta} \cdot \ell n \frac{1 + 2\delta(f - f_0)/(f_2 - f_1)}{1 - 2\delta(f - f_0)/(f_2 - f_1)} + V_0 \quad .$$

If the above is used instead of (3) to compute the objective function by (7) and (11), the resulting behavior of the modulation slope turns out to be closer to the acceptable one, defined by (13), despite of the larger deviation of the actual frequency-voltage characteristic from a straight line. This technique is usually very effective for broadbanding the linearizing network.

A design example

In this section we report about a varactor-tuned transistor oscillator that was designed according to the above method. The oscillator was devised to act as an extra-low-noise frequency-modulated source for a 120 voice channel FM radio link, with mechanically selected carrier frequency ranging from 2.3 to 2.43 GHz. The minimum required output power was 24 dBm throughout this band, and the acceptable deviation from FM linearity was 1% over ±3 MHz from the carrier. A modulation slope between 2 and 4 MHz/V was desired.

To meet the specifications on noise and output power, a brass coaxial cavity was used as the resonant circuit and was coupled to the base of a common-collector transistor via a capacitive coupling and a section of microstrip transmission line. Thus a circuit topology such as described in fig. 1 was realized. By using either a TRW 63601 or an MSC 80018 transistor an output power of about 25 dBm was measured across the operating band. In both cases the FM noise was less than 1 Hz r.m.s. over a 100 Hz band 14 KHz apart from the carrier. The tuning varactor mount and linearizing network as well as the oscillator circuit itself (except for the cavity) were built on 1.58 mm DUROID substrate by MIC techniques. The tuning network was parallel-connected to the microstrip line in a section some 90 degrees apart from the transistor base, roughly corresponding to a current node.

The measured B(f) and V(f) around centre-band (f_0= 2.365 GHz) were, for this circuit:

$$B(f) \simeq -28\pi f(f - f_0)\cdot 10^{-21} \text{ mho}$$

$$V(f) \simeq 20 \text{ V} \quad .$$

After performing a number of trial computations on different circuits, the topology schematically illustrated in fig. 3 was selected for the linearizing network.

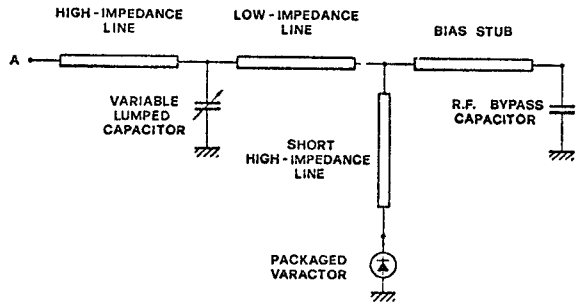

Fig. 3
Topology of linearizing network

In this network the short high-impedance line acts as a lumped inductance preventing the varactor capacitance from being resonated within the band of operation, while the low-impedance line plays an essential role in lowering the R.F. voltage across the varactor junction. The lumped variable capacitor was introduced for practical convenience, to provide compensation for the spread of the actual electrical parameters of the varactor with respect to the nominal ones used in the calculations. An ALPHA DKW 6533 F diode was computer-selected for this application in the way described in the previous section; the optimized bias voltage was 8.4 V.

The computed behavior of the optimized linearizing network is shown in fig. 4, where the applied D.C. voltage is plotted against frequency deviation from centre-band.

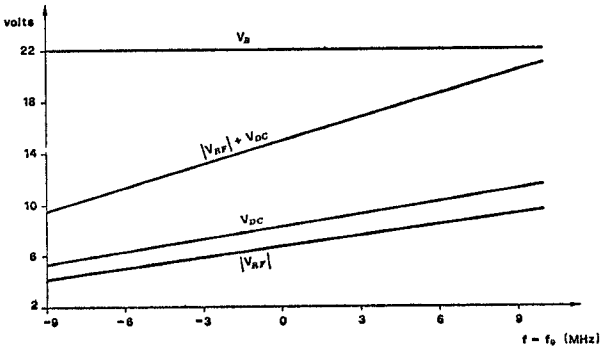

Fig. 4
Computed performance of linearizing network

From fig. 4 the frequency-voltage characteristic of the modulator is seen to be practically indistinguishable from a straight line over ±9 MHz from the carrier: the maximum relative error is actually 0.5% in this band. The resulting modulation slope is approximately 2.9 MHz/V at $f=f_0$.
The measured dependence of the modulation slope on frequency was found to be qualitatively of the form (13). Its percentage change was less than 1% over ±3.5 MHz from the carrier and less than 2% over ±4.7 MHz, in excellent agreement with the theoretical predictions.
The computed magnitude of the R.F. voltage across the junction is also plotted against frequency deviation in fig. 4 and is seen to be lower than the D.C. voltage by at least 1.2 V. Thus the diode appears to be protected from being driven into forward conduction. The same is true as breakdown is concerned, as the figure shows. Actually no forward conduction or breakdown effects were observed during the operation of the practical circuit.

A performance similar to that described above was obtained from the VTO over the whole band of mechanical tuning (2.3 ÷ 2.43 GHz).

Aknowledgement

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